Amendments to the Specification:

Please replace paragraph [0003] as follows:

[0003] This application is a continuation-in-part to U.S. Patent Application No. 08/956,740 filed on October 23, 1997, which issued on April 10, 2001 as U.S. Patent No. 6,215,778; which is a continuation of U.S. Patent Application No. 08/669,775 filed on June 27, 1996, which issued on August 25, 1998 as U.S. Patent No. 5,799,010; which claims the benefit of U.S. Provisional Application No. 60/000,775 filed on June 30, 1995. This application is also a continuation-in-part to U.S. Patent Application No. 09/003,104 filed on January 6, 1998, which issued on January 30, 2001 as U.S. Patent No. 6,181,949; which is a continuation of U.S. Patent Application No. 08/670,162 filed on June 27, 1996, which issued on November 24, 1998 as U.S. Patent No. 5,841,768. This application is also a continuation-in-part to U.S. Patent Application No. 09/304,286 filed on May 3, 1999, which issued on June 26, 2001 ~~August 19, 2003~~ as U.S. Patent No. 6,252,866 ~~6,608,825~~; which is a continuation of U.S. Patent Application No. 08/671,068 filed on June 27, 1996, which issued on August 17, 1999 as U.S. Patent No. 5,940,382. This application is also a continuation-in-part to U.S. Patent Application No. 09/354,042 filed on July 15, 1999, which issued on August 19, 2003 as U.S. Patent No. 6,608,825; which is a continuation of U.S. Patent Application No. 08/671,067 filed on June 27, 1996, which issued on September 14, 1999 as U.S. Patent No. 5,953,346. This application is also a continuation-in-part to U.S. Patent Application No. 09/129,580 filed on August 6, 1998, which issued on February 13, 2001 as U.S. Patent No. 6,187,424; which is a continuation of U.S. Patent Application No. 08/670,160 filed on June 27, 1996, which issued on November 26, 2002 as U.S. Patent No. 6,487,190. This application is also a continuation of U.S. Patent Application No. 09/079,600 filed on May 15, 1998, which issued on June 11, 2002 as U.S. Patent No. 6,405,272; which is a continuation of U.S. Patent Application No. 08/671,221 filed on June 27, 1996, which issued on May 19, 1998 as U.S. Patent No. 5,754,803.

Please replace paragraph [0096] as follows:

[0096] Figures 57A - 57E, taken together, are ~~Figure 57A-E is~~ an electrical schematic of an embodiment of the present invention.

On page 21, line 20, please change "STN" to "PSTN".

Please replace paragraph [0151] as follows:

[0151] The APC data rate is sent at 64 kbs. The APC logical channel is not FEC coded to avoid delay and is transmitted at a relatively low power level to minimize capacity used for APC. Alternatively, the APC and OW may be separately modulated using complex spreading code sequences or they may be time division multiplexed ~~multilplexed~~.

Please replace paragraph [0212] as follows:

[0212] Figure 3c shows the chip matched filter 301, matched to the chip waveform $P_{Tc}(t)$, and the sampler 302. Ideally, the signal $x(t)$ at the output terminal of the chip matched filter 301 is:

$$x(t)=\sum_{i=k}^{M}\sum_{k=-\infty}^{\infty}a_i c_k g(t-\tau_i-kT_c) \qquad \text{Equation (9)}$$

where:

$$g(t) = P_{Tc}(t)*h_R(t) \qquad \text{Equation (10)}$$

M is the number of multipath components. Here, $h_R(t)$ is the impulse response of the chip matched filter 301 and '*' denotes convolution. The order of the summations can be rewritten as:

$$\cancel{x(t)=\sum_{k=-\infty}^{\infty}c_k \int (t-kT_c)}$$

$$\underline{x(t)=\sum_{k=-\infty}^{\infty}c_k f(t-kT_c)} \qquad \text{Equation (11)}$$

where: $$\cancel{\int(t)=\sum_{i=1}^{M}a_i g(t-\tau_i)}$$

$$f(t)=\sum_{i=1}^{M}a_i g(t-\tau_i) \qquad \text{Equation (12)}$$

In the multipath channel described above, the sampler 302 samples the output signal of the chip matched filter 301 to produce x(nT) at the maximum power level points of *g(t)*. In practice, however, the waveform *g(t)* is severely distorted because of the effect of the multipath signal reception, and a perfect time alignment of the signals is not available.

Please replace paragraph [0213] as follows:

[0213] When the multipath distortion in the channel is negligible and a perfect estimate of the timing is available, i.e., a_1=1, $\underline{\tau_1=0}$ ~~t_1=0~~, and a_i=0, i=2,...,M, the received signal is *r(t)* = *s(t)*. Then, with this ideal channel model, the output of the chip matched filter becomes:

$$x(t)=\sum_{k=-\infty}^{\infty}c_k g(t-kT_c) \qquad \text{Equation (13)}$$

Please replace paragraph [0217] as follows:

[0217] Define τ to be the time estimate that the tracking circuit calculates during a particular sampling interval. Also, define the following error function as:

$$\varepsilon=\left\{\int_{\{t:|\tau-t|>\delta\}} f(t)dt \qquad |\tau-t|>\delta\right. \qquad \text{Equation (14)}$$

$$\varepsilon=0 \qquad |\tau-t|<\delta$$

The tracking circuits of the prior art calculate a value of the input signal that minimizes the error ε. One can write:

$$\cancel{\min\varepsilon=1-\max\tau\int_{\tau-\delta}^{\tau-\delta}f(t)}$$

$$\min\varepsilon=1-\max\tau\int_{\tau-\delta}^{\tau+\delta}f(t)\,dt \qquad \text{Equation (15)}$$

Please replace paragraph [0226] as follows:

[0226] Based on these observations, a realization of an exemplary tracking circuit which minimizes the squared weighted error is shown in Figure 5a. The following Equation (22) determines the error signal ~~e(t)~~ ε(τ) of the centroid tracking circuit:

$$\varepsilon(\tau)=\sum_{n=1}^{2L} n\left[\left|f(\tau-nT/2)\right|-\left|f(\tau+nT/2)\right|\right]=0 \qquad \text{Equation (22)}$$

The value that satisfies $\varepsilon(\tau)=0$ ~~$\varepsilon(t)=0$~~ is the perfect estimate of the timing.

Please replace paragraph [0228] as follows:

[0228] The weighted early multipath signal energy values are summed in sample adder 510 to give an output value proportional to the signal energy in the group of multipath signals corresponding to positive code phases which are the early multipath signals. Similarly, a second correlation bank adaptive matched filter 503 operates on the late samples, using the negative spreading code phases c(n-1), c(n-2), ..., c(n-L); each output signal is provided to a respective sum-and-dump circuit of discrete integrator 505. The magnitude value of the L sum-and-dump output signals are calculated by the respective calculator of calculator bank 507 and then weighted in weighting bank 509. The weighted late multipath signal energy values are summed in sample adder 511 to give an energy value for the group of multipath signals corresponding to the negative code phases which are the late multipath signals. Finally, the adder 512 calculates the difference of the early and late signal energy values to produce error sample value ~~$\varepsilon(t)$~~ $\varepsilon(\tau)$.

Please replace paragraph [0229] as follows:

[0229] The tracking circuit of Figure 5a produces error signal ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$ which is used to adjust the locally generated code phase c(nT) to keep the weighted average energy in the early and late multipath signal groups equal. The embodiment shown uses weighting values that increase as the distance from the centroid increases. The signal energy in the earliest and latest multipath signals is probably less than the multipath signal values near the centroid. Consequently, the difference calculated by the adder 510 is more sensitive to variations in delay of the earliest and latest multipath signals.

Please replace paragraph [0231] as follows:

[0231] In this embodiment of the tracking method, the tracking circuit adjusts the sampling phase to be "optimal" and robust to multipath. Let f(t) represent the received signal waveform as in Equation (12) above. The particular method of optimizing starts with a delay locked loop with an error signal ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$ that drives the loop. The function ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$ must have only one zero at $\tau=\tau_0$ where τ_0 is optimal. The optimal form for $\varepsilon(\tau)$ has the canonical form:

$$\varepsilon(\tau)=\int_{-\infty}^{\infty} w(t,\tau)|f(t)|^2\,dt \qquad \text{Equation (23)}$$

where $w(t,\tau)$ is a weighting function relating f(t) to the error $\varepsilon(\tau)$, and the relationship indicated by Equation (24) also holds:

$$\varepsilon(\tau+\tau_0)=\int_{-\infty}^{\infty} w(t,\tau+\tau_0)|f(t)|^2\,dt \qquad \text{Equation (24)}$$

Please replace paragraph [0233] as follows:

[0233] The error ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$ has a deterministic part and a noise part. Let z denote the noise component in ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$, then $|z|^2$ is the average noise power in the error function ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$. Consequently, the optimal tracking circuit maximizes the ratio

$$F = \frac{M^2}{|z|^2} \qquad \text{Equation (26)}$$

Please replace paragraph [0234] as follows:

[0234] The implementation of the quadratic detector is now described. The discrete error value ε of an error signal ~~$\varepsilon(t)$~~ $\underline{\varepsilon(\tau)}$ is generated by performing the operation

$$\varepsilon = y^T B y \qquad \text{Equation (27)}$$

where the vector y represents the received signal components yi, i = 0, 1, ... L-1, as shown in Figure 5b. The matrix B is an L by L matrix and the elements are determined by calculating values such that the ratio F of Equation (26) is maximized. The quadratic detector described above may be used to implement the centroid tracking system described above with reference to Figure 5a. For this implementation, the vector y is the output signal of the sum and dump circuits 504: y={f(τ-LT), f(τ-LT+T/2), f(τ-(L-1)T), . . . f(τ), f(τ+T/2), f(τ+T), . . . f(τ+LT)} and the matrix B is set forth in Table 9.

Please replace paragraph [0242] as follows:

[0242] An exemplary implementation of the pilot AVC used to despread the pilot spreading code is shown in Figure 7. The described embodiment assumes that the input signal x(τ) has been sampled with sampling period T to form samples x(nT+τ), and is composed of interference noise of other message channels, multipath

signals of message channels, thermal noise and multipath signals of the pilot code. The signal x(nT+τ) is applied to L correlators, where L is the number of code phases over which the uncertainty within the multipath signals exists. Each correlator 701, 702, 703 comprises a multiplier 704, 705, 706, which multiples the input signal with a particular phase of the pilot spreading code signal c((n+i)T) and sum-and-dump circuits 708, 709, 710. The output signal of each multiplier 704, 705, 706 is applied to a respective sum-and dump circuit 708, 709, 710 to perform discrete integration. Before summing the signal energy contained in the outputs of the correlators, the AVC compensates for the channel response and the carrier phase rotation of the different multipath signals. Each output of each sum-and-dump 708, 709, 710 is multiplied with a derotation phasor ~~phaser~~ [complex conjugate of ep(nT)] from digital phase lock loop (DPLL) 721 by the respective multiplier 714, 715, 716 to account for the phase and frequency offset of the carrier signal. The pilot rake AMF calculates the weighting factors wk, k=1, .., L, for each multipath signal by passing the output of each multiplier 714, 715, 716 through a low pass filter (LPF) 711, 712, 713. Each despread multipath signal is multiplied by its corresponding weighting factor in a respective multiplier 717, 718, 719. The output signals of the multipliers 717, 718, 719 are summed in a master adder 720, and the output signal p(nT) of the accumulator 720 consists of the combined despread multipath pilot signals in noise. The output signal p(nT) is also input to the DPLL 721 to produce the error signal ep(nT) for tracking of the carrier phase.

Please replace paragraph [0245] as follows:

[0245] Referring to Figure 8a, the input signal x(t) is sampled to form x(nT+τ) ~~x(nT+t)~~, and is composed of interference noise of other message channels, multipath signals of message channels, thermal noise, and multipath signals of the pilot code. The signal ~~x(nT+t)~~ x(nT+τ) is applied to L correlators, where L is the number of code phases over which the uncertainty within the multipath signals exists. Each correlator 801, 802, 803 comprises a multiplier 804, 805, 806, which multiples the

input signal by a particular phase of the message channel spreading code signal, and a respective sum-and-dump circuit 808, 809, 810. The output signal of each multiplier 804, 805, 806 is applied to a respective sum-and dump circuit 808, 809, 810 which performs discrete integration. Before summing the signal energy contained in the output signals of the correlators, the AVC compensates for the different multipath signals. Each despread multipath signal and its corresponding weighting factor, which is obtained from the corresponding multipath weighting factor of the pilot AVC, are multiplied in a respective multiplier 817, 818, 819. The output signals of multipliers 817, 818, 819 are summed in a master adder 820, and the output signal z(nT) of the accumulator 820 consists of sampled levels of a despread message signal in noise.

Please replace paragraph [0247] as follows:

[0247] A third embodiment of the adaptive vector correlator is shown in Figure 8c. The embodiment shown uses the least mean square (LMS) statistic to implement the vector correlator and determines the derotation ~~decoration~~ factors for each multipath component from the received multipath signal. The AVC of Figure 8c is similar to the exemplary implementation of the Pilot AVC used to despread the pilot spreading code shown in Figure 7. The digital phase locked loop 721 is replaced by the phase locked loop 850 having voltage controlled oscillator 851, loop filter 852, limiter 853 and imaginary component separator 854. The difference between the corrected despread output signal ido and an ideal despread output signal dos is provided by adder 855, and the difference signal is a despread error value ide which is further used by the ~~decoration~~ derotation circuits to compensate for errors in the ~~decoration~~ derotation factors.

Please replace paragraph [0251] as follows:

[0251] The combined multipath component signal y(t) does not include the correction due to phase and frequency offset of the carrier signal. The correction for the phase and frequency offset of the carrier signal is made to y(t) by multiplying y(t) with carrier phase and frequency correction (derotation phasor ~~phaser~~) in multiplier 878. The phase and frequency correction is produced by the AVC as described previously. Figure 8d shows the correction as being applied before the despreading circuits 880, but alternate embodiments of the invention can apply the correction after the despreading circuits.

Please replace paragraph [0303] as follows:

[0303] The auxiliary AVC 1712 also receives the I and Q digital receive message signal data and, in the described embodiment, includes four separate despreaders 2001, 2002, 2003, 2004 as shown in Figure 20. Each despreader receives and correlates the I and Q digital receive message data with delayed versions of the same despreading code sequence PARI and PARQ which are provided by code generator 1304 input to and contained in shift register 2020. The output signals of the despreaders 2001, 2002, 2003, 2004 are combined in combiner 2030 which provides noise correlation signal ARDSPRDAT. The auxiliary AVC spreading code sequence does not correspond to any transmit spreading code sequence of the system. Signals OE1, OE2, ...OE4 are used by the modem control 1303 to enable the despreading operation. The Auxiliary AVC 1712 provides a noise correlation signal ARDSPRDAT from which quantile estimates are calculated by the quantile ~~estimator~~ estimation logic 1733, and provides a noise level measurement to the ACQ & Track logic 1701 (shown in Figure 17) and modem controller 1303 (shown in Figure 13).

Please replace paragraph [0316] as follows:

[0316] Two sets of quantile statistics are maintained, one by the vector quantile estimation logic 1733 and the other by the scalar quantile ~~estimator~~ estimation logic 1723 ~~1723A~~. Both are used by the modem controller 1303. The first set is the "vector" quantile information, so named because it is calculated from the vector of four complex values generated by the AUX AVC receiver 1712. The second set is the scalar quantile information, which is calculated from the single complex value AUX signal that is output from the AUX despreader 1707. The two sets of information represent different sets of noise statistics used to maintain a pre-determined probability of false alarm (P_{fa}). The vector quantile data is used by the acquisition and reacquisition algorithms implemented by the modem controller 1303 to determine the presence of a received signal in noise, and the scalar quantile information is used by the code lock check algorithm.

Please replace paragraph [0329] as follows:

[0329] Table 12 - Example B Matrix

0	0	0	0	0	0	0	0	0	0	0
0	0	-0.1	0	0	0	0	0	0	0	0
0	-0.1	0.22	0.19	-0.19	0	0	0	0	0	0
0	0	0.19	1	0.45	-0.2	0	0	0	0	0
0	0	-0.19	0.45	0.99	0.23	0	0	0	0	0
0	0	0	-0.2	0.23	0	-0.18	0.17	0	0	0

0	0	0	0	0	-0.18	-0.87	-0.42	0.18	0	0
0	0	0	0	0	0.17	-0.42	-0.92	-0.16	0	0
0	0	0	0	0	0	0.18	-0.16	-0.31	0	0
0	0	0	0	0	0	0	0	0	-0.13	0
0	0	0	0	0	0	0	0	0	0	0

Code tracking is implemented via a loop phase detector that is implemented as follows. The vector y is defined as a column vector which represents the 11 complex output level values of the pilot AVC 1711, and B denotes an 11×11 symmetric real valued coefficient matrix with pre-determined values to optimize performance with the non-coherent pilot AVC output values y. The output ~~signal e~~ signal ε of the phase detector is given by Equation (42):

$$\cancel{e = y^T By} \quad \varepsilon = \mathrm{y}^{\mathrm{T}}\mathrm{By} \qquad \text{Equation (42)}$$

The following calculations are then performed to implement a proportional plus integral loop filter and the VCO:

~~x[n] = x[n-1] +be~~

$x[n] = x[n-1] + \beta\varepsilon$

~~z[n] = z[n-1] + x[n] +ae~~

$z[n] = z[n-1] + x[n] + \alpha\varepsilon$

for ~~b and a~~ β and α which are constants chosen from modeling the system to optimize system performance for the particular transmission channel and application, and where x[n] is the loop filter's integrator output value and z[n] is the

VCO output value. The code phase adjustments are made by the modem controller <u>in</u> the following C-subroutine:

```
if (z > zmx) {
delay phase 1/16 chip;
z -= zmax;
} else if (z < -zmax) {
advance phase 1/16 chip;
z += zmax;
}
```